

## WHAT IS CLAIMED IS:

1 *Sub*  
2 *a* 1. An M-bit adder capable of receiving a first M-bit  
3 comprising:

4 M adder cells arranged in R rows, wherein a least  
5 significant adder cell in a first one of said rows of adder cells  
6 receives a first data bit,  $A_x$ , from said first M-bit argument and  
7 a first data bit,  $B_x$ , from said second M-bit argument, and  
8 generates a first conditional carry-out bit,  $C_x(1)$ , and a second  
9 conditional carry-out bit,  $C_x(0)$ , wherein said  $C_x(1)$  bit is  
10 calculated assuming a row carry-out bit from a second row of adder  
11 cells preceding said first row is a 1 and said  $C_x(0)$  bit is  
12 calculated assuming said row carry-out bit from said second row is  
13 a 0.

1 2. The M-bit adder as set forth in Claim 1 wherein said  
2 least significant adder cell generates a first conditional sum bit,  
3  $S_x(1)$ , and a second conditional sum bit,  $S_x(0)$ .

1 *pat* 3. The M-bit adder as set forth in Claim 2 wherein said  
2  $S_x(1)$  bit is calculated assuming said row carry-out bit from said  
3 second row is a 1 and said  $S_x(0)$  bit is calculated assuming said  
4 row carry-out bit from said second row is a 0.

1 4. The M-bit adder as set forth in Claim 3 wherein said row  
2 carry-out bit selects one of said  $S_x(1)$  bit and said  $S_x(0)$  bit to  
3 be output by said least significant adder cell.

1 5. The M-bit adder as set forth in Claim 4 wherein said  
2 first row of adder cells further comprises a second adder cell  
3 coupled to said least significant adder cell, wherein said second  
4 adder cell receives a second data bit,  $A_{x+1}$ , from said first M-bit  
5 argument and a second data bit,  $B_{x+1}$ , from said second M-bit  
6 argument, and receives from said least significant adder cell said  
7  $C_x(1)$  bit and said  $C_x(0)$  bit.

1 *Pat* 6. The M-bit adder as set forth in Claim 5 wherein said  
2 second adder cell generates a first conditional carry-out bit,  
3  $C_{x+1}(1)$ , wherein said  $C_{x+1}(1)$  bit is generated from said  $A_{x+1}$  data bit,  
4 said  $B_{x+1}$  data bit, and said  $C_x(1)$  bit from said least significant  
5 adder cell.

1 7. The M-bit adder as set forth in Claim 6 wherein said  
2 second adder cell generates a second conditional carry-out bit,  
3  $C_{x+1}(0)$ , wherein said  $C_{x+1}(0)$  bit is generated from said  $A_{x+1}$  data bit,  
4 said  $B_{x+1}$  data bit, and said  $C_x(0)$  bit from said least significant  
5 adder cell.

1 8. The M-bit adder as set forth in Claim 7 wherein said  
2 second adder cell generates a first conditional sum bit,  $S_{x+1}(1)$ ,  
3 wherein said  $S_{x+1}(1)$  bit is generated from said  $A_{x+1}$  data bit, said  
4  $B_{x+1}$  data bit, and said  $C_x(1)$  bit from said least significant adder  
5 cell.

1 *Sub* 9. The M-bit adder as set forth in Claim 8 wherein said  
 2 *ai* second adder cell generates a second conditional sum bit,  $S_{x+1}(0)$ ,  
 3 wherein said  $S_{x+1}(0)$  bit is generated from said  $A_{x+1}$  data bit, said  
 4  $B_{x+1}$  data bit, and said  $C_x(0)$  bit from said least significant adder  
 5 cell.

10. The M-bit adder as set forth in Claim 9 wherein said row  
 carry-out bit selects one of said  $S_{x+1}(1)$  bit and said  $S_{x+1}(0)$  bit to  
 be output by said second adder cell.

11. The M-bit adder as set forth in Claim 1 wherein said  
 first row of adder cells contains N adder cells and said second row  
 of adder cells preceding said first row contains less than N adder  
 cells.

1 *Sub*  
2 *Pat*  
12. A data processor comprising:

3 an instruction execution pipeline comprising N processing  
4 stages, each of said N processing stages capable of performing one  
5 of a plurality of execution steps associated with a pending  
6 instruction being executed by said instruction execution pipeline,  
7 wherein at least one of said N processing stages comprises an M-bit  
8 adder capable of receiving a first M-bit argument, a second M-bit  
9 argument, and a carry-in (CI) bit, said M-bit adder comprising:

10 M adder cells arranged in R rows, wherein a least  
11 significant adder cell in a first one of said rows of adder  
12 cells receives a first data bit,  $A_x$ , from said first M-bit  
13 argument and a first data bit,  $B_x$ , from said second M-bit  
14 argument, and generates a first conditional carry-out bit,  
15  $C_x(1)$ , and a second conditional carry-out bit,  $C_x(0)$ , wherein  
16 said  $C_x(1)$  bit is calculated assuming a row carry-out bit from  
17 a second row of adder cells preceding said first row is a 1  
18 and said  $C_x(0)$  bit is calculated assuming said row carry-out  
bit from said second row is a 0.

1 *Sub* 13. The data processor as set forth in Claim 12 wherein said  
2 least significant adder cell generates a first conditional sum bit,  
3  $S_x(1)$ , and a second conditional sum bit,  $S_x(0)$ .

1 14. The data processor as set forth in Claim 13 wherein said  
2  $S_x(1)$  bit is calculated assuming said row carry-out bit from said  
3 second row is a 1 and said  $S_x(0)$  bit is calculated assuming said  
4 row carry-out bit from said second row is a 0.

1 15. The data processor as set forth in Claim 14 wherein said  
2 row carry-out bit selects one of said  $S_x(1)$  bit and said  $S_x(0)$  bit  
3 to be output by said least significant adder cell.

1 16. The data processor as set forth in Claim 15 wherein said  
2 first row of adder cells further comprises a second adder cell  
3 coupled to said least significant adder cell, wherein said second  
4 adder cell receives a second data bit,  $A_{x+1}$ , from said first M-bit  
5 argument and a second data bit,  $B_{x+1}$ , from said second M-bit  
6 argument, and receives from said least significant adder cell said  
7  $C_x(1)$  bit and said  $C_x(0)$  bit.

1 *Sub* 17. The data processor as set forth in Claim 16 wherein said  
2 second adder cell generates a first conditional carry-out bit,  
3  $C_{x+1}(1)$ , wherein said  $C_{x+1}(1)$  bit is generated from said  $A_{x+1}$  data bit,  
4 said  $B_{x+1}$  data bit, and said  $C_x(1)$  bit from said least significant  
5 adder cell.

1 18. The data processor as set forth in Claim 17 wherein said  
2 second adder cell generates a second conditional carry-out bit,  
3  $C_{x+1}(0)$ , wherein said  $C_{x+1}(0)$  bit is generated from said  $A_{x+1}$  data bit,  
4 said  $B_{x+1}$  data bit, and said  $C_x(0)$  bit from said least significant  
5 adder cell.

1 19. The data processor as set forth in Claim 18 wherein said  
2 second adder cell generates a first conditional sum bit,  $S_{x+1}(1)$ ,  
3 wherein said  $S_{x+1}(1)$  bit is generated from said  $A_{x+1}$  data bit, said  
4  $B_{x+1}$  data bit, and said  $C_x(1)$  bit from said least significant adder  
5 cell.

1 *sub* 20. The data processor as set forth in Claim 19 wherein said  
2 *part* second adder cell generates a second conditional sum bit,  $S_{x+1}(0)$ ,  
3 wherein said  $S_{x+1}(0)$  bit is generated from said  $A_{x+1}$  data bit, said  
4  $B_{x+1}$  data bit, and said  $C_x(0)$  bit from said least significant adder  
5 cell.

1 21. The data processor as set forth in Claim 20 wherein said  
2 row carry-out bit selects one of said  $S_{x+1}(1)$  bit and said  $S_{x+1}(0)$   
3 bit to be output by said second adder cell.

1 22. The data processor as set forth in Claim 12 wherein said  
2 first row of adder cells contains N adder cells and said second row  
3 of adder cells preceding said first row contains less than N adder  
4 cells.



*Pat*  
23. A method of adding a first M-bit argument and a second M-bit argument in an M-bit adder, the M-bit adder comprising M adder cells arranged in R rows, the method comprising the steps of:

receiving a first data bit,  $A_x$ , from the first M-bit argument and a first data bit,  $B_x$ , from the second M-bit argument in a least significant adder cell in a first one of the rows of adder cells;

calculating in the least significant adder cell a first conditional carry-out bit,  $C_x(1)$ , assuming a row carry-out bit from a second row of adder cells preceding the first row is a 1;

calculating in the least significant adder cell a second conditional carry-out bit,  $C_x(0)$ , assuming the row carry-out bit from the second row is a 0;

calculating in the least significant adder cell a first conditional sum bit,  $S_x(1)$ , assuming the row carry-out bit from the second row is a 1;

calculating in the least significant adder cell a second conditional sum bit,  $S_x(0)$ , assuming the row carry-out bit from the second row is a 0;

propagating the  $C_x(1)$  bit and the  $C_x(0)$  bit to a second adder cell in the first row of adder cells; and

selecting one of the  $S_x(1)$  bit and the  $S_x(0)$  bit to be

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**PATENT**

~~output from the least significant adder cell according to a value of the row carry-out bit from the second row.~~

1277 1272 1268 1244 1237 1231 1227 1222 1219 1214 1210 1206 1202 1198 1194 1190 1186 1182 1178 1174 1170 1166 1162 1158 1154 1150 1146 1142 1138 1134 1130 1126 1122 1118 1114 1110 1106 1102 1098 1094 1090 1086 1082 1078 1074 1070 1066 1062 1058 1054 1050 1046 1042 1038 1034 1030 1026 1022 1018 1014 1010 1006 1002 998 994 990 986 982 978 974 970 966 962 958 954 950 946 942 938 934 930 926 922 918 914 910 906 902 898 894 890 886 882 878 874 870 866 862 858 854 850 846 842 838 834 830 826 822 818 814 810 806 802 798 794 790 786 782 778 774 770 766 762 758 754 750 746 742 738 734 730 726 722 718 714 710 706 702 698 694 690 686 682 678 674 670 666 662 658 654 650 646 642 638 634 630 626 622 618 614 610 606 602 598 594 590 586 582 578 574 570 566 562 558 554 550 546 542 538 534 530 526 522 518 514 510 506 502 498 494 490 486 482 478 474 470 466 462 458 454 450 446 442 438 434 430 426 422 418 414 410 406 402 398 394 390 386 382 378 374 370 366 362 358 354 350 346 342 338 334 330 326 322 318 314 310 306 302 298 294 290 286 282 278 274 270 266 262 258 254 250 246 242 238 234 230 226 222 218 214 210 206 202 198 194 190 186 182 178 174 170 166 162 158 154 150 146 142 138 134 130 126 122 118 114 110 106 102 98 94 90 86 82 78 74 70 66 62 58 54 50 46 42 38 34 30 26 22 18 14 10 6 2